Electronic Version
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Claims

[c1] What is claimed is:

1. A network interface circuit for transmitting signals to different nodes of a network, the network interface circuit comprising:

a first scrambler for generating a first transmission signal by executing a logic operation with a first signal and a first scrambling code;

a second scrambler for generating a second transmission signal by executing the logical operation with a second signal and a second scrambling code, wherein the first scrambling code and the second scrambling code are different such that the first transmission signal and the second transmission signal are unlike; and

two transmission ports for transmitting the first and the second transmission signals to the corresponding network nodes.

[c2] 2. The network interface circuit of claim 1 whereinthe first scrambler comprises a first random number generator for executing a second logic operation with a first seed to generate the first scrambling code, and the second scrambler comprises a second random number gen-

erator for executing the second logic operation with a second seed to generate the second scrambling code; wherein the first seed and the second seed are different so that the first scrambling code and the second scrambling code are unlike.

[c3] 3. The network interface circuit of claim 2 capable of updating the value of the first seed after a predetermined period after the first scrambler generates the first transmission signal, and capable of updating the value of the second seed after the predetermined period after the second scrambler generates the second transmission signal.

[c4] 4.The network interface circuit of claim 3 in which the first scrambler generates the first transmission signal after receiving a first reset signal, and the second scrambler generates the second transmission signal after receiving a second reset signal, wherein the first reset signal and the second reset signal are transmitted to the first scrambler and the second scrambler respectively at different times so that the first scrambler and the second scrambler start to generate the first transmission signal and the second transmission signal respectively at different times.

[c5] 5. The network interface circuit of claim 4 capable of

setting an initial value to the first seed when the first scrambler receives the first reset signal and another initial value to the second seed when the second scrambler receives the second reset signal.

[c6] 6. The network interface circuit of claim 1 further comprising a first encoder and a second encoder for encoding the first transmission signal and the second transmission signal respectively in the same way, the encoded first transmission signal and the encoded second transmission signal being transmitted to the corresponding network nodes through the two transmission ports, wherein the first encoder and the second encoder encode a signal composed of 0 and 1 values to one composed of 0, 1, and 1 values.

[c7] 7. The network interface circuit of claim 1 in which the logical operation is exclusive OR.

[c8] 8. A network interface circuit for transmitting signals to different nodes of a network; the network interface circuit comprising:
a reset circuit for generating a first reset signal and a second reset signal;
a first signal circuit comprising at least a first scrambler and generating a first transmission signal by utilizing the first scrambler to execute a logical operation with a first

signal and a first scrambling code when receiving a first reset signal;

a second signal circuit comprising at least a second scrambler and generating a second transmission signal by utilizing the second scrambler to execute the logical operation with a second signal and a second scrambling code when receiving a second reset signal; and

two transmission ports for transmitting the first and the second transmission signals to the corresponding network nodes.

[c9] 9. The network interface circuit of claim 8 in which the reset circuits generate the first reset signal and the second reset signal at different times so that the time of the first signal circuit to generate the first transmission signal and the time of the second signal circuit to generate the second transmission signal are not the same.

[c10] 10. The network interface circuit of claim 8 in which the first scrambler and the second scrambler are different so the first transmission signal and the second transmission signal are different even when the first signal is equal to the second signal.

[c11] 11. A method for a network interface circuit to transmit signals to different nodes of a network, the method

comprising:

executing a logical operation with a first signal and a first scrambling code, and executing the logical operation with a second signal and a second scrambling code, wherein the second scrambling code is different with the first scrambling code so the first transmission signal and the second transmission signals are different even when the first signal is equal to the second signal; and

transmitting the first transmission signal and the second transmission signal to the corresponding nodes of the network respectively.

[c12] 12. The method of claim 11 in which the first scrambling code is generated by executing a second logical operation with a first seed and the second scrambling code is generated by executing the second logical operation with a second seed, wherein the first seed and the second seed are different so that the first scrambling code and the second scrambling code are unlike.

[c13] 13. The method of claim 12 in which the value of the first seed is updated after a predetermined period after the first transmission signal is generated, and the value of the second seed is updated after the predetermined period after the second transmission signal is generated.

[c14] 14. The method of claim 13 in which the first transmis-

sion signal is generated after receiving a first reset signal, and the second transmission signal is generated after receiving a second reset signal, wherein the first reset signal and the second reset signal turn on the process of generating the first scrambling code and the process of generating the second scrambling code at different times, so that the first transmission signal and the second transmission signal are generated at different times.

[c15] 15. The method of claim 14 in which the first seed is set to an initial value when the first reset signal is received, and the second seed is set to another initial value when the second reset signal is received.

[c16] 16. The method of claim 11 capable of encoding the first transmission signal and the second transmission signal respectively in the same way, the encoded first transmission signal and the encoded second transmission signal being transmitted to the corresponding network nodes through the two transmission ports, the way of encoding is to encode a digital signal composed of 0 and 1 values to one composed of 0, 1, and 1 values.

[c17] 17. The method of claim 11 in which the logical operation is exclusive OR.

[c18] 18. A method for a network interface circuit to transmit

signals to different nodes of a network,
the method comprising:
receiving a first reset signal and a second reset signal;
executing a logical operation with a first signal and a first scrambling code to generate a first transmission signal right after receiving the first reset signal, and executing the logical operation with a second signal and a second scrambling code to generate a second transmission signal right after receiving the second reset signal, wherein the second transmission signal are different from the first transmission signal; and
transmitting the first transmission signal and the second transmission signal to the corresponding nodes in the network respectively.

[c19] 19. The method of claim 18 generating the first reset signal and the second reset signal at different times respectively so that the times to generate the first transmission signal and the second transmission signal are different.

[c20] 20. The method of claim 19 in which the first scrambling code and the second scrambling code are different so that the first transmission signal are not equal to the second transmission signal even when the first signal and the second signal are the same.